Luis Cupido, CT1DMK

Frequency Counter with Harmonic Mixing for the UHF/SHF Amateur

Taken from an address given to the VHF/UHF/SHF Technical Congress '94 in Munich

Amateurs building their own radio-frequency assemblies and equipment always need at least a minimum amount of measurement and testing equipment. This is particularly true for SHF operators, where there is not much measurement equipment available and prices are high. The frequency meter described below can measure up to 26.5 GHz (or even 33 GHz) with a resolution of 100 Hz, and with a constant sensitivity of - 10 dBm.

1. INTRODUCTION

It is well-known that there are reasonably-priced, ready-to-operate frequency counters which operate at up to 1.3 GHz. However, additional measurement equipment is required for the increasing levels of activity above 1.3 GHz.

A number of different procedures are available for frequency determination - e.g., using wave meters, cavity resonators and downwards converters with a known local oscillator frequency. These techniques can provide results which can certainly be of use. But because of the poor resolution, in particular for the downwards conversion procedure, they are not very practical for a receiver.

1.1. Brief Description of Frequency Measurement Procedure

Several procedures can be used to measure frequencies (only the essentials are dealt with here).

- Low frequencies (anything below 10 MHz) can be measured by counting the number of periods over a fixed time (1 second for a resolution of 1 Hz). This procedure is described as the direct counting procedure (TTL-LS and CMOS technologies can be used).

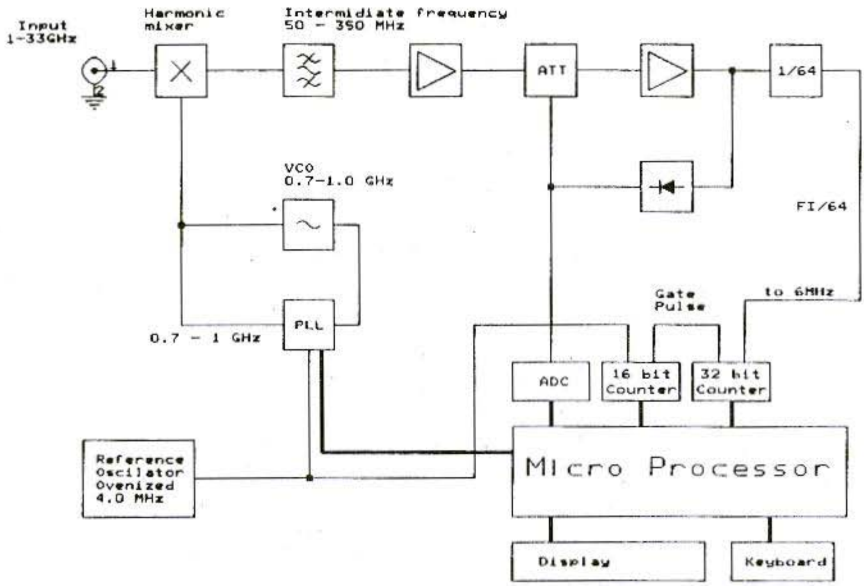


Fig.1: Block Diagram of a Frequency Counter with Harmonic Mixing

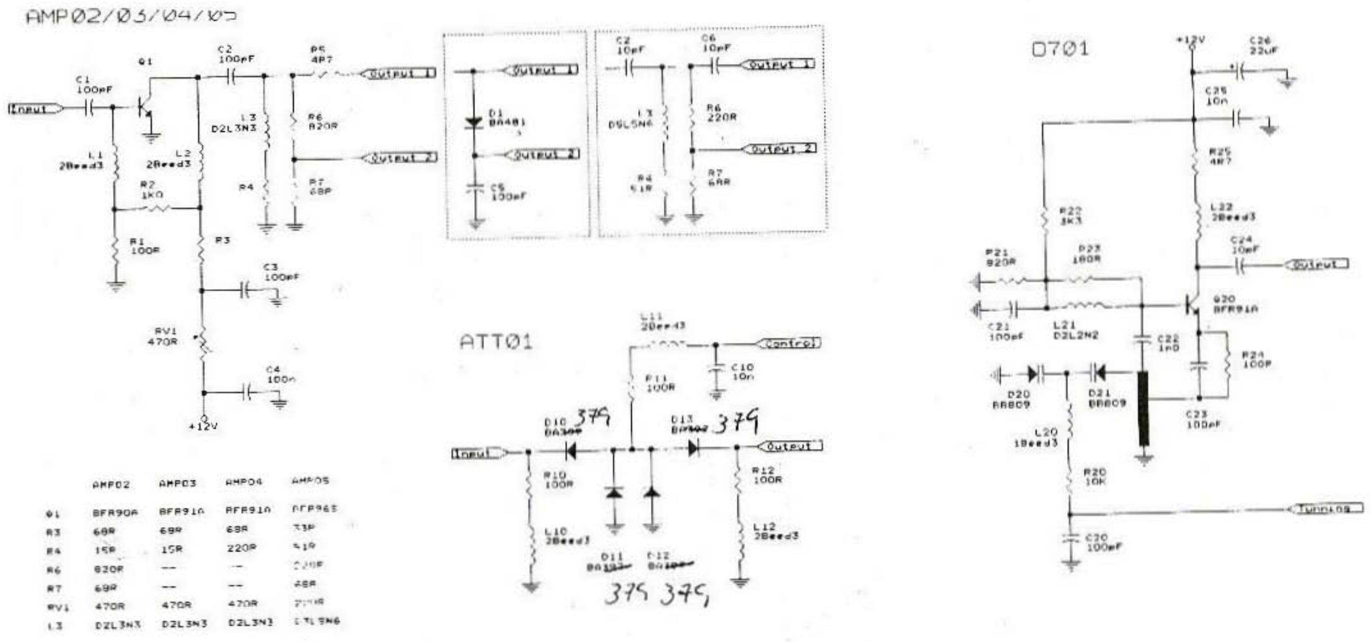
- For measurements at high frequencies, the range of direct-counting frequency counters can be expanded through the use of a pre-divider using ECL technology, with which the input frequency is divided by a factor, in general, of 10, 100, 64, 128 or 256. This procedure can be used only up to the maximum operating frequency of the divider used. Although 14-GHz pre-dividers are available on the market, they are very expensive and are beyond the reach of amateurs. Cheap pre-dividers do exist, with which division can be carried out at up to 2.5 GHz. However, most of them are for dynamic operation only - i.e. laid out as from a minimum operating frequency, so that they can be used for only a few bands.

- Frequency measurements on microwaves can be carried out with the help of wave meters and cavity resonators at low resolution.

Measurements using the counting procedure are possible only if the signal is converted to a lower intermediate frequency, which can then be measured by direct counting. This can be done using the following procedure:

1. Interference method using a simple superheterodyne receiver to measure the precise oscillator frequency and the intermediate frequencies.

2. Transfer oscillator procedures using a simple superheterodyne receiver with an oscillator linked to the intermediate frequency signal which is in a constant relationship with the frequency of the first oscillator, which is then measured.



	AMP02	AMP03	AMP04	AMP05
Q1	BFR90A	BFR91A	BFR91A	BFR96S
R3	68R	68R	68R	33R
R4	15R	15R	220R	51R
R6	820R	---	---	220R
R7	68R	---	---	68R
RV1	470R	470R	470R	[illegible]
L3	D2L3N3	D2L3N3	D2L3N3	D3L5N6

Note: Coils are air spaced with D diameter, L length and with N turns, or are N turns 3mm ferrite beads (2Bead3 = 2 turns on 3mm bead)

Fig.2: Assemblies 02, 03, 04 and ATT01

3. Harmonics procedure using a superheterodyne receiver with a harmonic mixer being used as a first mixer, so that very high frequencies can be converted to an intermediate frequency. The number of harmonics then also has to be calculated to determine the frequency of the measured signal.

1.2. Frequency Meter as per Harmonic Mixing Principle

This principle was selected for the microwave frequency counter, in particular, because it is the only principle which can be used to measure high frequencies using cheap components and local (first) oscillators (1. LO) below 1 GHz, which can easily be assembled by any experienced amateur.

The radio-frequency section of the counter consists of a harmonic mixer and the intermediate frequency section (see block diagram, Fig.1). To carry out the measurement, the first oscillator is swept through until a strong intermediate-frequency signal appears. The first oscillator is then locked and the intermediate frequency is measured and stored. The first oscillator is then stepped up by a small amount (e.g. 1 kHz) and the intermediate frequency is measured again to calculate the intermediate frequency shift and the direction of deviation. The ordinal number of the harmonic can then be determined by dividing the LO shift by the intermediate frequency shift (e.g. if the shift is 12 kHz then n = 12/1 = 12).

The conversion side band can be determined by examining the direction of the intermediate-frequency deviation (if downwards: USB, if upwards: LSB).

Finally, the measured frequency, f, amounts to:

$$f = LO \pm f_{IF}$$

The procedure described presupposes that a computer-controlled frequency counter is available. However, nowadays micro-controllers are simple to use and are sufficiently powerful to carry out the calculations for our applications.

2. CIRCUIT DESCRIPTION

The circuits are certainly extensive. But they are not difficult to construct. Nor do they pose any special calibration problems. The equipment is built up from several existing assemblies - OSC2's, AMP02/03/04's and ATT01's.

2.1. The Harmonic Mixer

The harmonic mixer uses a BAT14 mixing diode (26-GHz version, with no leads) in a single-cycle circuit. This GaAs diode is controlled by a 17-dBm signal from the first oscillator in the 700 - 1,000 MHz range.

The rapid switching characteristics of the BAT14 make it possible to convert up to the 33rd harmonic of the oscillator with a mixing loss of app. 50 dB. The maximum efficiency of the harmonic mixer is essentially dependent on its structure. The maximum operating fre-

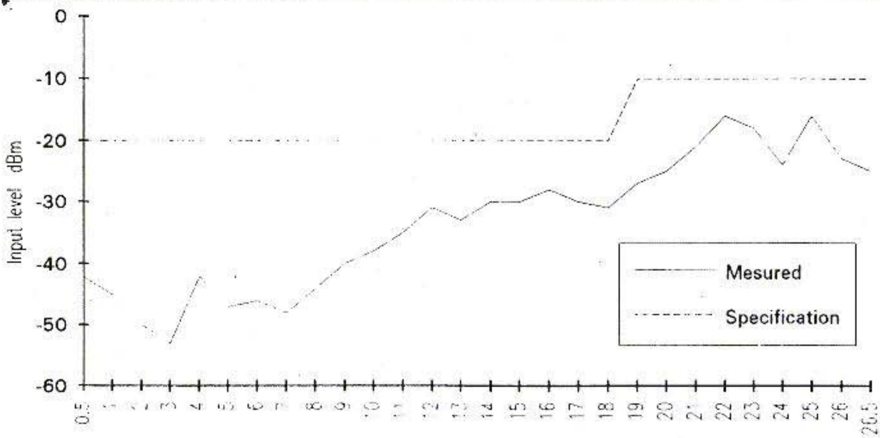


Fig.3: Characteristics of a BAT14 Diode: Comparison of Specification and Measured Values

Freq.	Sens.	Spec.
0.5	-42	-20
1	-45	-20
2	-50	-20
3	-53	-20
4	-42	-20
5	-47	-20
6	-46	-20
7	-48	-20
8	-44	-20
9	-40	-20
10	-38	-20
11	-35	-20
12	-31	-20
13	-33	-20
14	-30	-20
15	-30	-20
16	-28	-20
17	-30	-20
18	-30	-20
19	-27	-10
20	-25	-10
21	-21	-10
22	-16	-10
23	-18	-10
24	-24	-10
25	-16	-10
26	-23	-10
26.5	-25	-10

Frequency Meter I/P Sensitivity using a BAT14 diode as harmonic mixer

quency of the equipment is also determined by the upper operating frequency of the harmonic mixer. The structure of the harmonic mixer is described later.

2.2. The Intermediate-Frequency Pre-Amplifier

In the preamplifier, the main emphasis has been laid on a low noise factor within the intermediate frequency range and on maximum suppression of the LO frequency, which is extremely undesirable in the intermediate-frequency circuits. This assembly comprises a Chebycheff bandpass filter, followed by two AMP02 amplifiers, with an amplification of more than 25 dB in the intermediate-frequency range of 50 - 350 MHz. The amplifier assemblies use BFR90A transistors. At the output of the second amplifier, a signal weakened by - 10 dB is decoupled to an external intermediate-frequency output, which can be very useful.

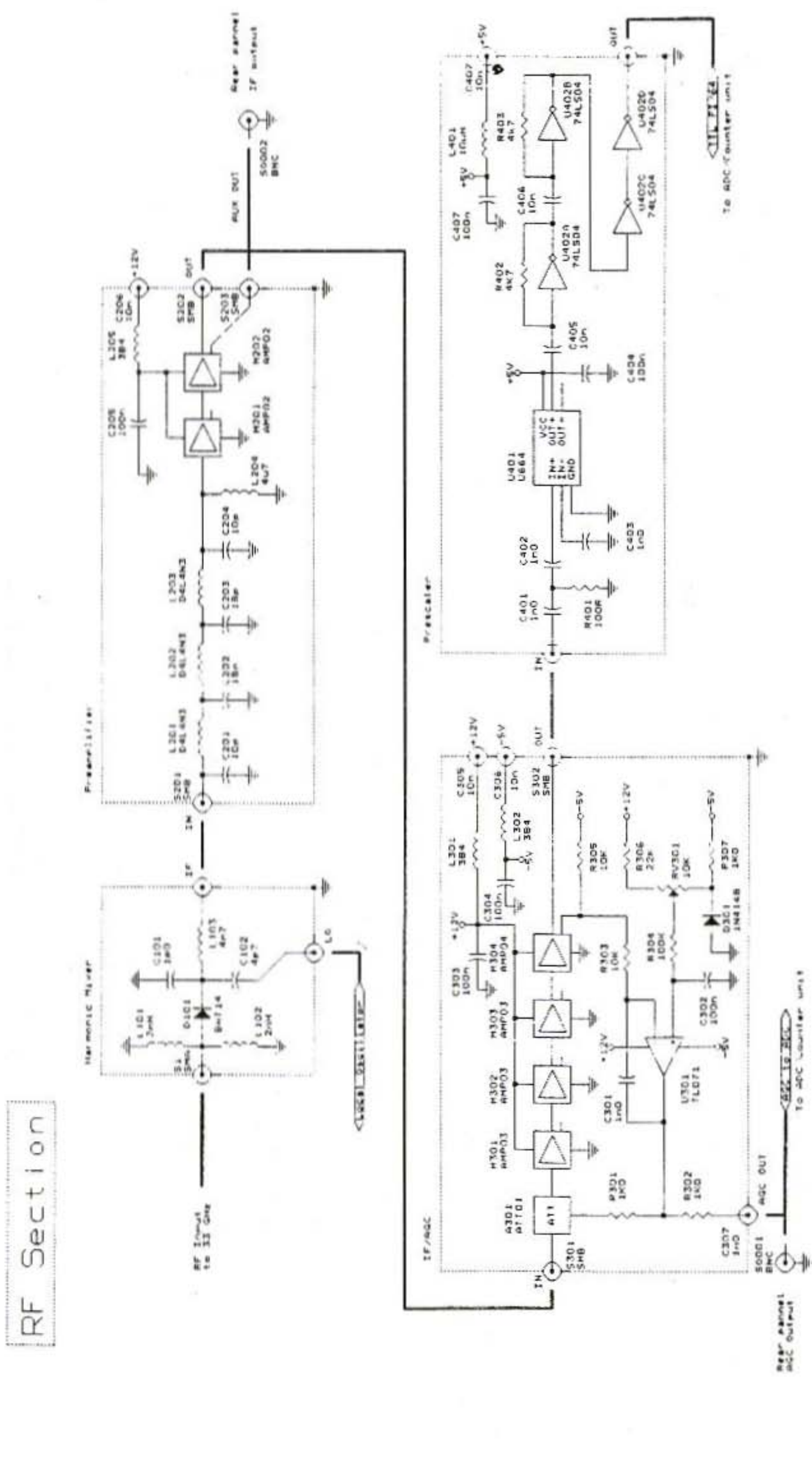


Fig.4: Circuit of Mixer, Preamplifier, IF/AGC and Pre-Divider

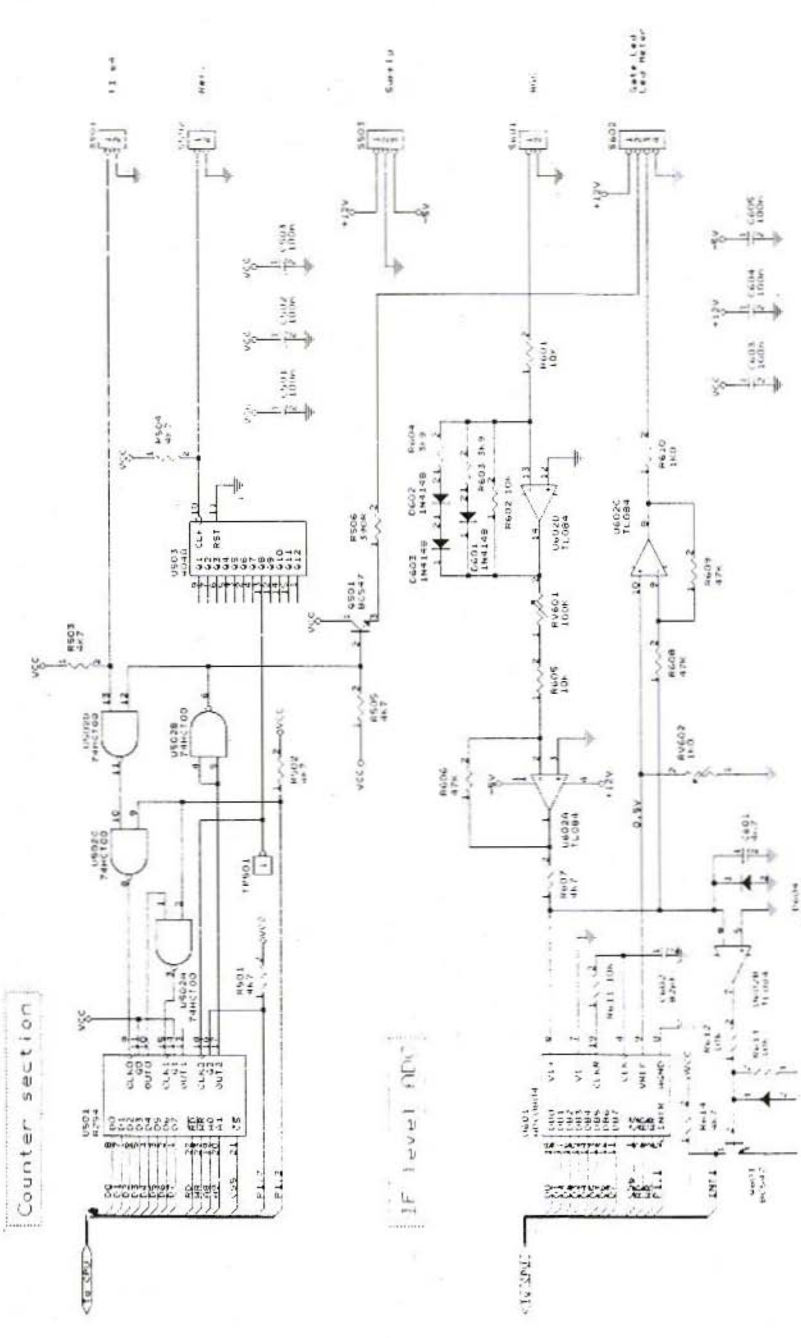


Fig.5: Circuit of Counter Section and IF Analogue/Digital Converter

2.3. The Intermediate-Frequency Amplifier And AGC

In this stage, the signal supplied by the preamplifier is amplified to the level of 0 dBm required for the processing in the subsequent digital circuits. The intermediate-frequency amplifier is 4-stage, built for a total amplification of more than 45 dB. To maintain a constant output level, the final stage contains an AGC detector to control the AGC circuits. This amplifier must have a flat frequency response in the 50 - 350 MHz range and should have as little noise as possible, so as to improve the operating threshold of the subsequent digital circuits.

The dynamic range of this intermediate frequency naturally has to be greater than the dynamic range which would be desirable for any kind of input frequency. The reason for this lies in the fact that the mixed attenuation of the harmonic mixer changes from 7 dB to 50 dB for the higher harmonics.

The best operating results for the frequency counter could be achieved if the intermediate-frequency amplifier had so much total amplification that a noise signal would be supplied at its output which was so high that it could be processed directly by the digital circuits. This happens at a level of approximately - 10 to 0 dBm. at the input of the next stage.

Signals above the noise are counted, although the dynamic range of the ECL input to the next stage is narrow. So it is desirable to have a constant-level signal available at the output of the intermediate-frequency section for every signal at a level which is considerably higher than the noise level. This is brought about by an automatic gain control (AGC), which operates over a wide range and makes good level compensation possible.

Signal limiters or limiter amplifiers are not desirable here, as to a large extent they generate harmonics which can impair the digital circuit functions. Remember, that with an intermediate-frequency signal of 50 MHz the harmonics are in the 50 - 350 MHz measurement range. The AGC's wide dynamic range is obtained through the control of a PIN-diode attenuating element with which over 70 dB of attenuation can be attained.

The AGC circuit is very simple and effective. Here the intermediate-frequency level is compensated using a DC current (adjusted at RV301), so that the comparator (also used as an integrator) closes the control loop through the attenuating element. The AGC's response time is in the order of 10 ms.

The AGC signal is fed into the m..... processor for the intermediate-frequency level to be evaluated. An LED column display provides an indication of the signal level, derived from the AGC signal.

2.4. The Pre-Divider

This part of the circuit serves only to bring the intermediate frequency to a level which lies within the operating range of digital CMOS circuits. Only an ECL divider from Telefunken is used in the circuit (others could have been used as well). The pre-divider is supplied with a 0 dBm signal and

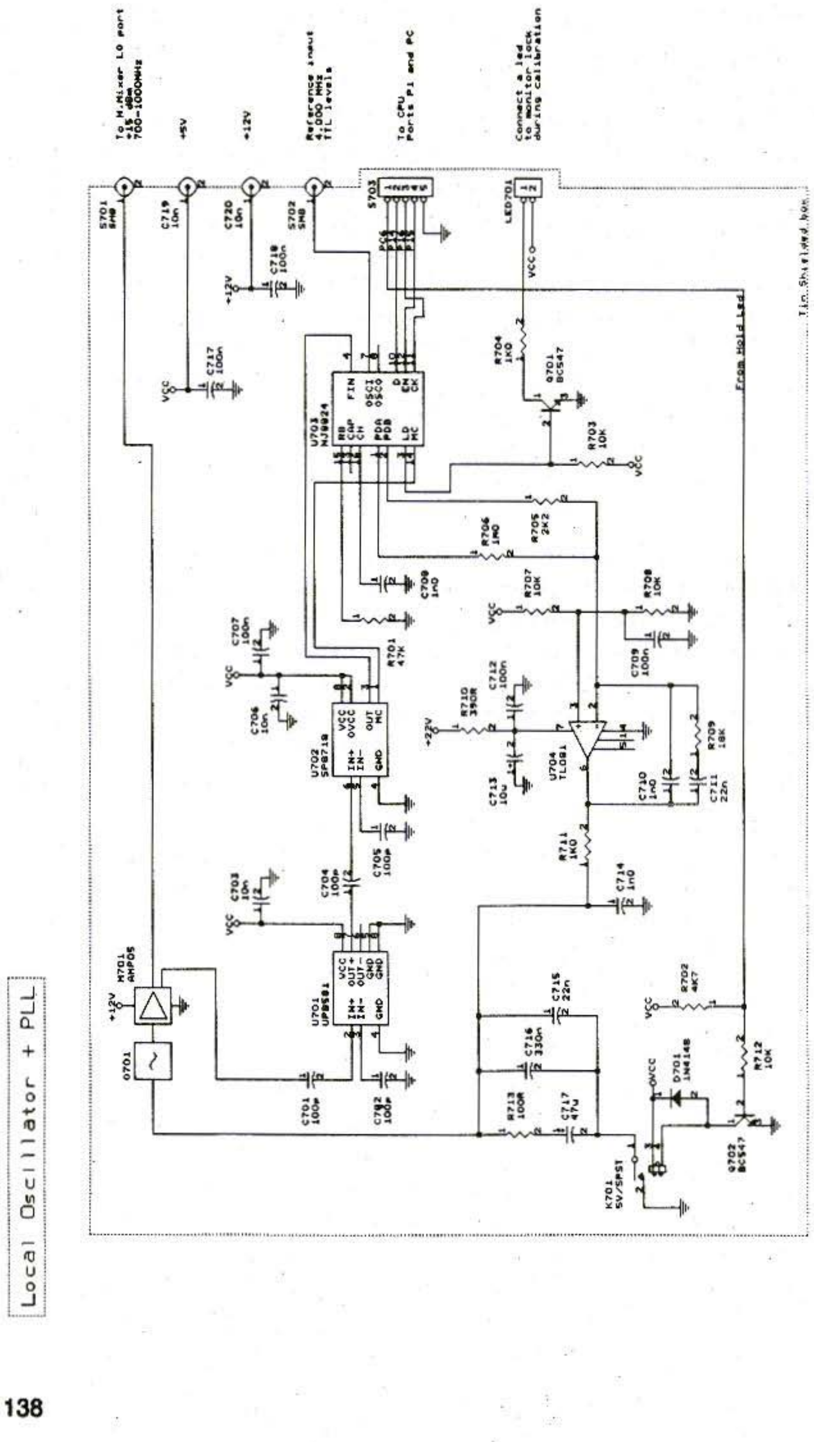


Fig.6: Circuit of LO and PLL assemblies

divides by 64. A TTT-LS inverter converts the signal to the TTL level.

2.5. The Counter Section

Here the intermediate-frequency signal, already divided, is fed to an Intel 8254 (3x16 bit counter), which is directly controlled by the micro-processor. Counters 0 and 1 are cascaded to make a 32-bit counter resolution possible, whilst counter 2 is used as a one-shot for the input gate control. The micro-processor controls all 3 counters directly.

The reference frequency for controlling the highly precise trigger signal is generated by dividing a 4-MHz signal which is supplied by a thermostatically-stabilised crystal oscillator, which is not mounted on the printed circuit board.

2.6. Analogue/Digital Conversion of Intermediate-Frequency Level

The AGC signal is initially processed in an analogue circuit to improve the real range of the AD converter (remember that the attenuating element in the intermediate frequency/AGC branch displays a very strongly non-linear attenuation gradient). Additional components are needed to send a signal to the micro-processor in case of saturation.

2.7. The First (Local) Oscillator

The first oscillator has to supply a high-level high-frequency signal (+ 17 dBm) to control the harmonic mixer.

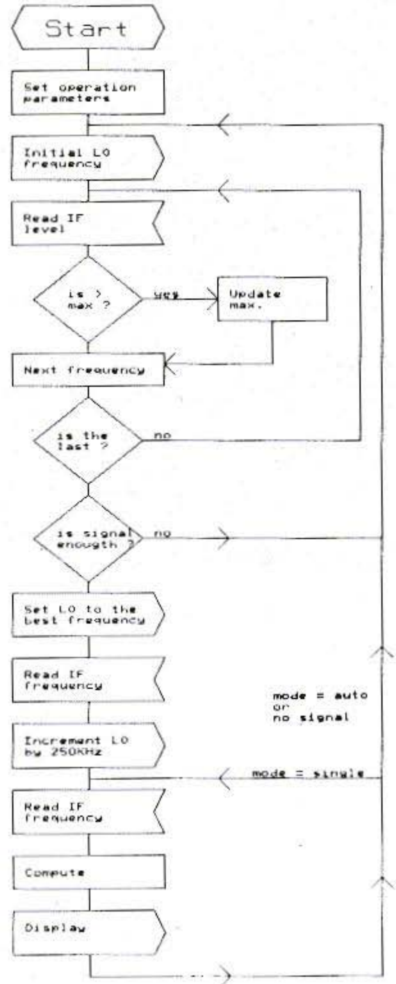


Fig.7: Flow Diagram of Software needed for Freq. Counter

The oscillator, the frequency of which can be varied over a wide range, uses a micro-strip transmission circuit. It is followed by an amplifier which supplies the output level required.

One part of the oscillator signal, attenuated by 20 dB by a PB581C pre-

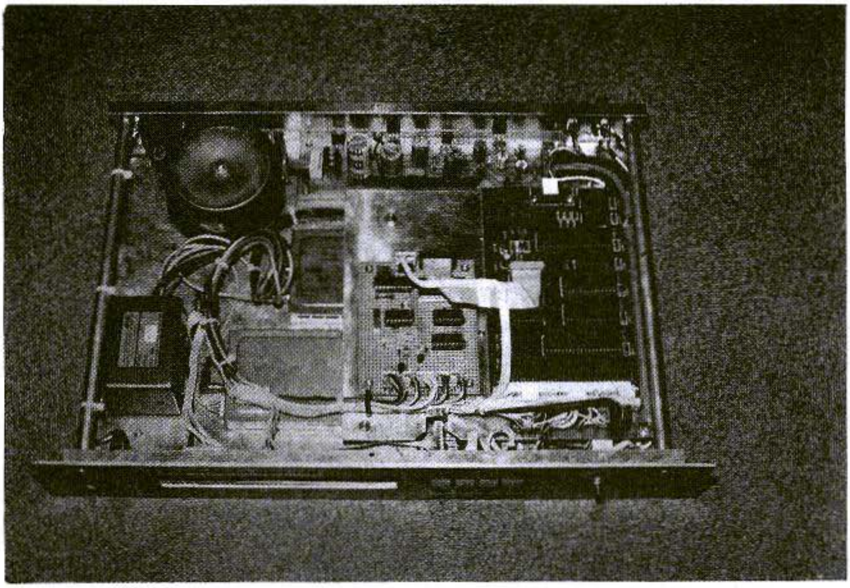


Fig.8: The Prototype unit with the easily identifiable CPU Board

divider, is fed to a dual-mode SP8727 pre-divider, which is controlled by a PLL-IC NS8242.

The NS8242 PLL module (Plessey) is a dual-mode PLL-IC with serial control inputs and two phase detectors. Motorola modules can also be used, but software changes are required.

The PLL-IC uses the same external reference signal of 4 MHz as the counter section. In the loop filter, an OP amplifier is used in the classic way. In addition, a considerably narrower filter can be wired up, if the user selects the count dwell period to obtain a considerably purer LO spectrum. Because of this characteristic, the frequency counter can be used as a reception converter.

An LED is provided to light up when the PLL is engaged. But this is needed only for the testing and calibration procedures.

2.8. The Micro-Controller

Control and frequency counting require this equipment to have functions involving the making of decisions and fixed point calculations with 32-bit resolution. This makes it absolutely necessary to use a micro-controller.

A programmable 8032 board generally obtainable from component suppliers, R.S, etc., is used as micro-controller. This board has an 8031 with an RS232 interface, an 8255 PPI, an 8-k RAM and a 16-k ROM. 100% compatible boards can be set up how you like, provided the following addressing data are included:

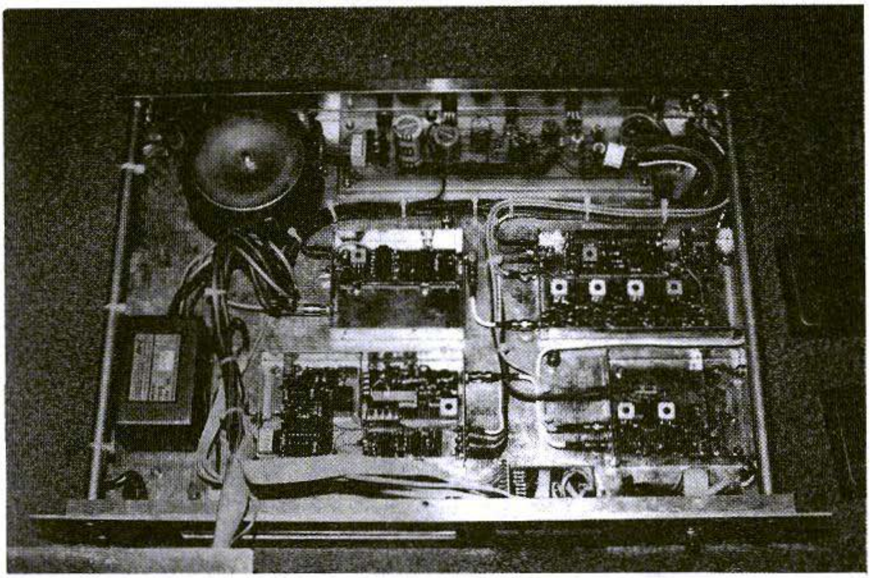


Fig.9: The Lower Assemblies are mounted in tin-plate housings on the base

ROM address:	000H...400H
RAM address:	800H...A000H
8255-PPI address:	E000/E100/E200 and E300H
CS5:	A000H
CS6:	B000H

CS5 and CS6 are used in the intermediate-frequency level and counting assemblies.

In the switching documents, you will find the descriptions P1.0 to P1.7, corresponding to port P1 of the 8031, whilst ports PA0 to PA7 and PB0 to PB7 (reserved for the "reference source connection" option) and PC0 to PC7 correspond to ports A, B and C of the 8255 interface module (this is all you need to know). Commercially obtainable boards can be used.

2.9. The Software

The software required for controlling this frequency meter must include the sequences laid down in the flow chart (Fig.7). As well as a computer core, it must also have interfaces to the user, so that mode and resolution can be selected.

In this context, the requirement for simple operation has controlled the development of the software, but without this leading to too great a loss of flexibility. It goes beyond the scope of this article to describe or illustrate the various software development options, or to provide the software listings, which are over 10 pages long. The software was developed using C language and takes up less than 8 kB of a ROM in its compiled form.

Important note: the software imposes no limit on the highest frequency available or on the number of harmonics, but only on the number of (display) characters displayed to the user - i.e., if anyone finds a harmonic mixer which, for example, displays a reasonable mixing loss at 76 GHz, then the counter will function well (I myself have tested it at 48 GHz).

3. ASSEMBLY

Assembly should not pose too many problems for an experienced amateur, as the most critical section operates on UHF frequencies using techniques with which most amateurs are familiar. The harmonic mixer, preamplifier, intermediate-frequency section, PLL and pre-divider should be individually screened. Coaxial plugs (SMB, SMC or SMA) should be used to connect up the assemblies. Power leads should always run through feedthrough capacitors. All this is normal practice for radio-frequency assembly.

3.1. The Harmonic Mixer

As this is the most critical assembly, it was built directly onto the back of a gold-plated SMA jack with a rectangular flange. The components are soldered to one another without feed wires, all within an area of 2 x 2 mm. on the earth side of the flanged bush. All components are in SMD format and the capacitors should display low losses at microwave frequencies. ATC types are recommended. The input inductors consist of 1.5 turns of 0.2 mm. gold wire, on a 1-mm. diameter core. If a good diode and a small format are chosen, results can be obtained up to 40 GHz.

3.2. The Pre-Amplifier

Two AMP02 amplifier blocks with BFR90A transistors are used in the preamplifier The filter has to attenuate the oscillator frequency by more than 70 dB, so it should be carefully assembled. Good screening is just as important as the filter itself here.

3.3. The IF/AGC Assembly

The attenuating element and the 4 amplifier stages of the intermediate-frequency amplifier are simply assembled one behind another in a shielded box, together with a specimen printed circuit board (2 x 5 cm.) for the AGC circuit. Normal radio-frequency assembly techniques should be used.

3.4. The Pre-Divider

A specimen printed circuit board can be used. The levels applied are 0 dBm in the 50 - 350 MHz range. Normal radio-frequency assembly techniques should be used.

3.5. The First Oscillator and the PLL

The first oscillator, consisting of an OSC2 stage, uses a BFR91A. It is directly followed by an amplifier stage

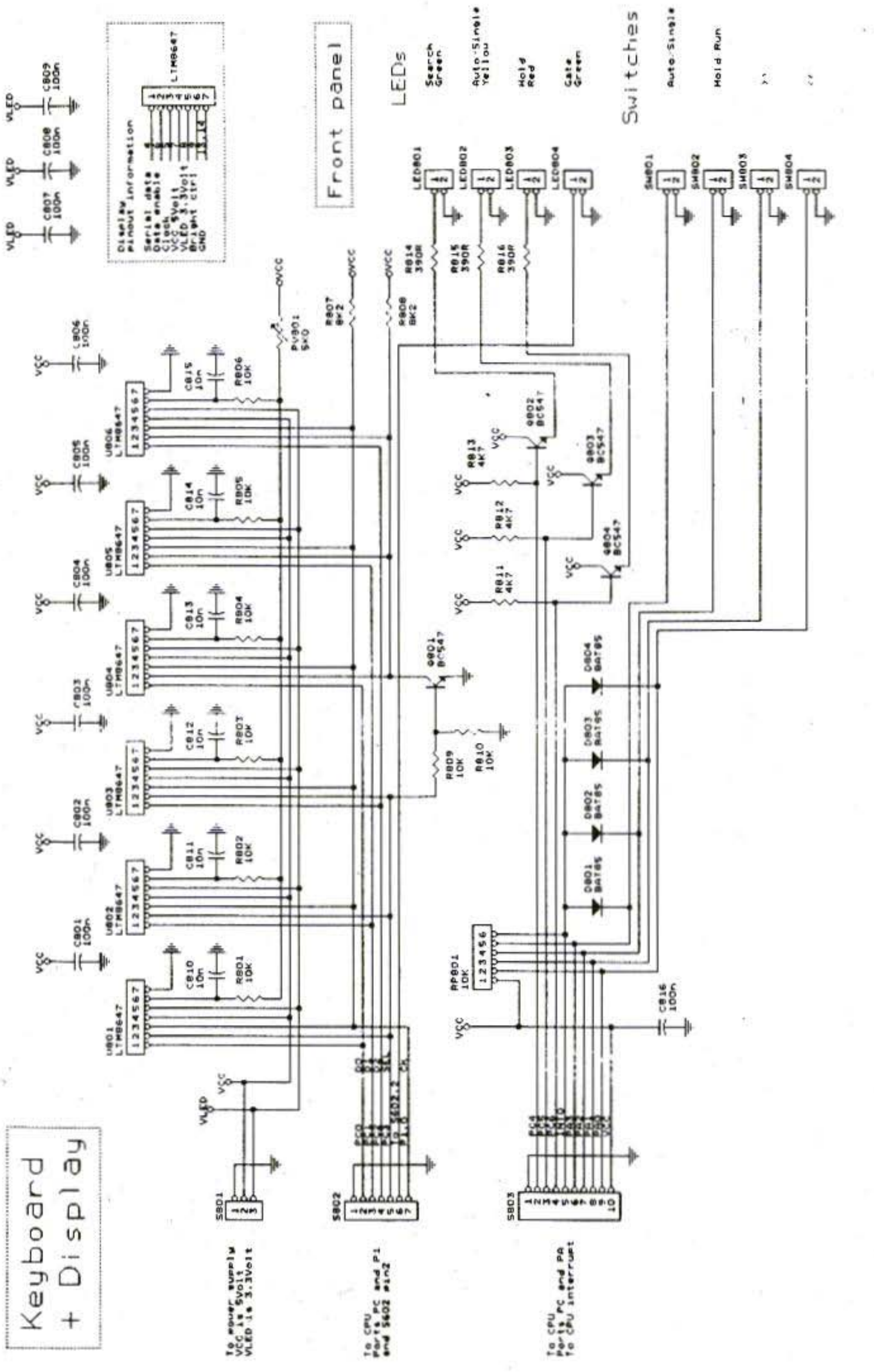


Fig.10: Circuit of the Keyboard and Display Unit

with the BFR96S. Good SMD capacitors should be used here. The predivider, the PLL-IC and the OP amplifier OPAMP are assembled on the surface of a standard board to produce a good earth connection. A shielding plate should be provided between the oscillator, the amplifier and the digital circuits.

3.6. The Counter and IF Level/AD Converter Assembly

Only high-level low-frequency signals are used in this assembly, so that it can be constructed using normal printed circuit boards or wire-wrap technology.

3.7. The Keyboard and Display Assembly

This can be built up however you like on the front panel. No critical circuits are used (Fig.10).

3.8. The Master Oscillator

Various oscillator circuits can be found in the literature. However, for optimal operation a thermostat-stabilised oscillator is recommended. Surplus units can also be very suitable.

3.9. The Power Supply

The requirements for operating this frequency counter are simple: + 12 V/0.35 A, + 5 V/0.6 A, - 5 V/25 mA, + 24 V/5 mA. This article does not describe the power supply.

4. TESTING AND CALIBRATION

Once the equipment has been assembled and the power supply voltages have been checked, the equipment can be powered up. It should be apparent that the software has started to operate immediately, and a start message should appear on the display unit. Any malfunctions occurring at this stage may be due to wrong connections on the micro-processor or interface module side or to damaged modules, for example in the ROM or the RAM. At all events, no further help can be given here. In the next stage, the PLL/first oscillator function is checked, as it is independent of the other radio-frequency sections. Equipment for measuring the power and frequency in the range between 0.5 and 1.5 GHz is needed here.

4.1. PLL/First Oscillator Test

The tuning voltage should be isolated from the oscillator and checked by means of an external power source or a variable resistance. During tuning between 1 and 20 V, a minimum tuning range of 650 - 1.050 MHz should be attained, and the output level should be at least 0 dBm. This level can be set with the help of the trimming resistor in the bias voltage circuit of the AMP05 amplifier. Monitor the temperature of the BFR96S during this test. The tuning voltage is then re-connected to the original circuit. As the program is running, the counter is in search

mode - i.e. the control voltage should sweep the oscillator through. A saw-tooth signal should be observed at pin-6 of the TL081.

4.2. Pre-Amplifier Testing

A preamplification of more than 25 dB and a 50 - 350 MHz band width should be measured in this assembly. No special test procedure is called for. The preamplifier can be optimised by setting the trimming resistor at any stage.

4.3. IF/AGC Testing

A spectrum analyser is of great use in the calibration of the intermediate frequency/AGC stage. The assembly is connected to a spectrum analyser. The RV301 trimming resistor should be turned up to maximum (in the direction of the R306 resistance). This causes the attenuating element to display the lowest level of attenuation. The total amplification for all stages should then be app. 48 dB. Calibrating each individual stage then improves the amplification and phase behaviour. Make sure that the gain slope and the output noise are constant over the 50 - 350 MHz range. The coils in each stage should be re-adjusted to obtain a flat gradient.

The input of the intermediate-frequency section is then connected to a radio-frequency generator at 150 MHz and at an output level of - 60 dBm. The signal level is then raised until a 0 dBm signal appears at the output. The RV301 trimming resistor is then slowly adjusted until the AGC responds. Monitor the AGC voltage gradient while the input level is being raised, with the output level remaining constant at 0 dBm. It should then be possible to observe a dynamic range of more than 60 dB. This testing can be repeated in the 50 - 350 MHz range for confirmation purposes.

4.4. Pre-Divider

Connect the pre-divider to the intermediate-frequency section and use the radio-frequency generator in the same way as when testing the intermediate-frequency section in AGC mode. The pre-divider output should always supply a clean square-wave signal.

4.5. The Counter Assembly

This assembly does not need calibrating. Only the gate pulse should be observed. When not in search mode, it should display steep flanks if the equipment is functioning correctly.

4.6. IF Level/AD Converter

This stage should be set in such a way that it supplies 0 - 1 V at the AD converter input. This is obtained by adjusting RV601 over the full AGC range. I recommend that the radio-frequency generator should be left connected to the intermediate-frequency section and the radio-frequency output should be switched on and off. When no radio-frequency signal is applied, a voltage of 1.050 V should be observed at pin-6 of the IC U601. For the adjustment of RV602, the reference voltage of the AD converter should be set to 0.5 V.

4.7. Final Test

Assuming that nothing has gone wrong, the frequency counter should now be capable of operating. The sensitivity of the equipment can now be checked with the help of a calibrated meter. If something is wrong:-

If the frequency counter does not operate satisfactorily, you should be in a position to identify the problem.

If the unit searches for a signal but never locks on, the most probable reasons are:

Non-functioning of AGC, no binary output signals on AD converter or no intermediate-frequency signal (harmonic mixer not working).

If the unit searches for a signal and locks on, but the display data varies between wide margins, the wiring in the counter section or the CPU section is incorrect, or something is wrong with the reference signal.

If the unit's functions collapse and are no longer available for operation, the wiring of the digital section should be checked.

5. OPERATION

Only 4 keys are used to operate the frequency counter. In the format described, the frequency counter is laid out for fully automatic operation and the user has only to select the resolution and the mode.

The keys > and < are provided for converting the resolution from 100 Hz to 1 MHz.

The "Search" key switches between automatic search per measurement and one search cycle per measurement. In the automatic search mode, the frequency counter goes into the search mode after each counting procedure. In the individual mode, the frequency counter searches and, if it finds something, it continues to count until the signal disappears.

The "Hold" key holds the display and the narrow-band lock mode of the PLL is set. In this mode, the equipment can be used as a receiver input stage.

6. CONCLUSIONS

Several improvements are being worked on at the moment and if relevant they will be made public at a later date. The prototype has now been working for a year, retaining the original specifications. Most components are wired up on specimen printed circuit boards or are in a wire-wrap format. Any co-operation or any joint effort to simplify the reproducibility would be interesting. I am also interested in hearing any observations concerning this project.

My special thanks go to DJ1CR, Max Munich, who was responsible for the selection of BAT14, which made it possible for me to obtain the optimum characteristics from this equipment.